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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,406	01/31/2001	Keizo Morita	1117.65148	3851

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EXAMINER	
WORKU, NEGUSSIE	
ART UNIT	**PAPER NUMBER**
2626	4

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/774,406	MORITA ET AL.	
	Examiner	Art Unit	
	Negussie Worku	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshiro Aoki (US Patent Application Publication No.2002/0047838).

With respect to claim 1, Aoki et al. discloses a display device (fig 1 shows a planar structure of a display device) comprising: a display section (display section 6 of fig 6) with scanning lines (scanning line 3 of fig 6); a scanning driver (scanning line driver 8 of fig 6) including output lines supplying scanning signals to said scanning said display section (display section 6 of fig 6); a judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) judging as whether each said scanning signals (scanning line 3 of fig 6) supplied from said scanning driver (driver 8 of fig 6, see col.6, paragraph 0068) and outputting the judging result; and a switching unit (pad 32 of fig 6, as switching unit is set to switch the voltage level V off,

see col.7 of last 6 lines of paragraph 0078) disconnecting the output line for supplying a scanning signal that said judging unit has judged as being defective, from the corresponding scanning line said display section (display section SR of fig 6, see col.7, paragraph 0076).

With respect to claim 2, Yoshiro Aoki et al. discloses the device (shown in fig 1-6) wherein said judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) judges as whether least said output said scanning driver fixed at ground potential, see (col.7, paragraph 0075 and paragraph 0078) and when said judging unit (a scan line test section 30 (35) of fig 6) has judged that least one said output lines said scanning driver (scanning driver 8 of fig 6) fixed said ground potential, switching (pad 32 of fig 6, as switching unit, set to the voltage level V off, see col.7 of last 6 lines of paragraph 0078) disconnects fixed output from the corresponding scanning line of said display section (display section SR of fig 6).

With respect to claim 3, Aoki et al. discloses the device wherein said judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) judges as whether or not at least one of said output lines said scanning driver (8 of fig 6) fixed at a power supply potential, (supplying a power to scanning drive 8 of fig 1, is inherent) and when said judging unit (30 935) of fig 6) has judged that at least one of said output lines said scanning driver (8 of fig 6) is fixed at said power supply potential

said switching unit (pad 32 of fig 6) disconnects the fixed output line from the corresponding scanning line said display section (display section SR of fig 6).

With respect to claim 4, Aoki et al. discloses the device (shown in fig 1-6) wherein said judging unit (a scan line test section 30 (35) of fig 6) judges as whether least one said output lines said scanning driver (8 of fig 6) disconnected, and, when said judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) has judged that at least one of said output lines of said scanning driver (8 of fig 6) disconnected, said switching unit (pad 32 of fig 6, switching and set to the needed voltage level) disconnects the disconnected output line from the corresponding scanning line of said display section (display section SR of fig 6).

With respect to claim 5, Aoki et al. discloses the device (shown in fig 1-6) wherein said switching unit (pad 32 of fig 6) disconnects said output lines said scanning driver (scanning driver 8 of fig 6) from all said scanning lines said display section (SR of fig 6) when said judging unit (30 935) of fig 6) has judged that least two neighboring output lines said scanning driver (8 of fig 6) are defective (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6).

With respect to claim 6, Aoki et al. discloses the device (shown in fig 1-6) wherein said judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6), comprises a check transistor with gate, source and drain,

see col.6, lines 0068 of the last 5 lines) said gate receiving a signal corresponding the scanning signal on an output line of said scanning driver (scanning driver 8 of fig 60 and a judging section (a scan line test section 30 (35) of fig 6) for checking as whether not check signal is transmitted between said source and drain of said check transistor in response said signal supplied said gate said check transistor, see (col.6, paragraph 0068 of fig 6) so as judge as to whether or not said scanning signal said output line of said scanning driver defective (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6).

With respect to claim 7, Aoki et al. discloses the device (shown in fig 6) wherein said gate of said check transistor (transistors 35 of fig 6, as a check (testing transistor), see col.6, of the last line) is connected to said output line of said scanning driver (8 of fig 6).

With respect to claim 8, Aoki et al. discloses the device wherein judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line) further comprises an AND circuit (8A of fig 4) for performing an AND operation relation the said check transistor (transistors 35 of fig 6, as a check (testing transistor), see col.6, of the last line) connected said scanning signals on two neighboring output lines said scanning driver, (8 of fig 6) said AND circuit (8A of fig 3) having its output connected said gate said check transistor (35 of fig 6).

With respect to claim 9, Aoki et al. discloses the device (as shown in fig 6) switching unit (switching elements are transistors 5 of fig 6 see col.10, paragraph 0102 of last lines) comprises a transistor disconnecting an output line said from corresponding scanning line (scanning line 3 of fig 6) of said display section (display section SR of fig 6).

With respect to claim 10, Aoki et al. discloses the device (shown in fig 6) wherein said switching unit (transistors 5 of fig 6) comprises a CMOS transistor, see col.6, paragraph 0061 of last 5 lines) made up from an n-channel MOS transistor (Yn-Xm scan line (channel) and a p-channel MOS transistor said scanning driver (8 of fig 6) from the disconnecting an output line corresponding scanning line said display (SR of fig 6) section.

With respect to claim 11, Aoki et al. discloses the device (as shown in fig 1-6) the gate of said n-channel MOS transistor (5 of fig 6) is supplied with an out put of said judging unit, (a scan line test section 30 (35) of fig 6) the gate of said P-channel Mos transistor is supplied with the logically inverted of said output of said Judging unit, (a scan line test section 30 (35) of fig 6) and source and the drain of said n- and p-channel MOS transistors are connected to said output line of aid scanning driver (scan driver 8 of fig 6) and said scanning line of said display section (display area of fig 6).

With respect to claim 12, Aoki et al. discloses the device (as shown in fig 1-6) wherein said display section, (SR display section of fig 6) said scanning driver, (8 of fig 6) said judging unit, (35 of fig 6) said switching unit (5 of fig 6) are integrated single substrate (substrate 100 of fig 1, see col.3, paragraph 0033 of line 3-5).

With respect to claim 13, Aoki et al. discloses the device (as shown in fig 1) wherein said substrate device (100 of fig 1) said display section (SR of fig 6) comprises glass substrate (substrate 100 includes a transparent glass 102 of fig 2, see col.3, lines 0034).

With respect to claim 14, Aoki et al. discloses the display device (as shown in fig 6) wherein said display section (display area SR of fig 6) comprises a transistor, (35 of fig 6) and each said transistor said display section, (SR of fig 6) said check transistor said judging and transistor said switching unit (5 of fig 6), poly-silicon thin-film transistor (5T of fig 1, see col.14-17, of paragraph 0034).

With respect to claim 15, Aokia et al. discloses the device (shown in fig 1-6) wherein said display section has data lines, (display area SR of fig 6, has scan (data) line 3 of fig 6) said device further comprises first second data drivers (8 and 9 of fig 6) connected said data lines (data or scan line 3 and 4 of fig 6) of said display section supplying data signals said display section (display section SR of fig 6).

With respect to claim 16, Aokia et al. discloses the device (as shown in fig 1-6) further comprising: data signal judging unit (35 of fig 6) for judging as to whether or not the data signal supplied from of said first and second data drivers (8 and 9 of fig 6) judging least defective, (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6), and outputting judging result, (through out put buffer 8a of fig 4) and a data line for switching unit (switch 5 of fig 6) for disconnecting the supplying data signal that said data signal judging unit (30 [35] of fig 6) has Judged being defective, (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) from the corresponding data line said display section (display area SR of fig 6).

With respect to claim 17, Aoki et al. discloses the device (as shown in fig 1-6) wherein said display section (display area SR of fig 6) has data lines (scan line 3 and 4 of fig 6), and said device further comprises a data driver (signal or data line driver) connected said data lines said display section (SR display section of fig 6) for supplying data signals to said display section (display area SR of fig 6).

With respect to claim 18, Aoki et al. discloses the device (as shown in fig 6) wherein said data driver (6 of fig 6) comprises first data driver section (8 of fig 6) for supplying data signals some said data lines of said display section, (display area SR of fig 6) and second data driver section (9 of fig 6) supplying data signals the other of said data lines said display section (display area SR of fig 6).

With respect to claim 19, Aoki et al. discloses a liquid crystal display panel (LCD device of fig 1) filled with liquid crystal material between a pair of substrates, see (col.3, paragraph 0033) comprising: display section (display area SR of fig 6) with scanning lines (scanning line 3 of fig 6); scanning driver (8 of fig 6) including output lines for supplying scanning signals said scanning lines said display section (display area SR of fig 6); judging unit (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) for judging as whether not pair substrates each scanning judging said scanning signals supplied from said driver is defective, (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6) and outputting the result; and switching unit (switching unit 5 of fig 6) disconnecting output line supplying a scanning signal that said judging unit (30 [35] of fig 6) judged being defective, from corresponding scanning of said display section (display area SR of fig 6).

With respect to claim 20, Aoki et al. discloses a driving method a display device (shown in fig 1-6) comprising display section (display area SR of fig 6) with scanning lines, (scanning line 3 and 4 of fig 6) scanning driver (scanning driver 8 of fig 6) including output supplying scanning signals said scanning of said display section, (SR of fig 6) said method comprising steps judging as whether or each said scanning signals supplied from said scanning driver defective, (a scan line test section 30 (35) of fig 6 detects a defect of scanning line driver 8 of fig 6); and disconnecting the output supplying scanning signal that has been judged as being defective, see (col.4,

paragraph 0043 of lines 4-5, from corresponding scanning line said display section (display section SR of fig 6).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Negussie Worku whose telephone number is 305-5441. The examiner can normally be reached on 7am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached on 703-305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Negussie Worku
10/25/04

KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER